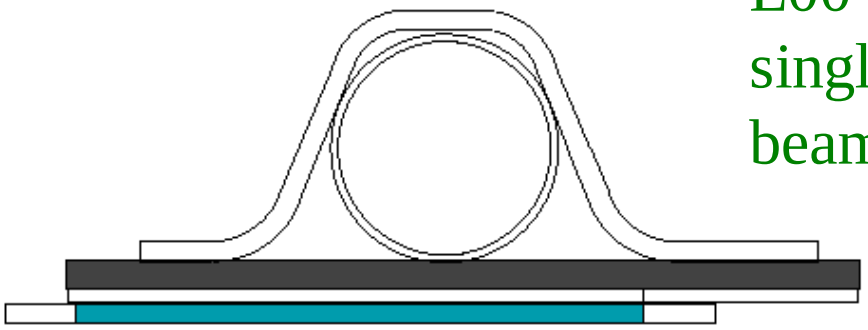
Pixels for CDF in Run IIb

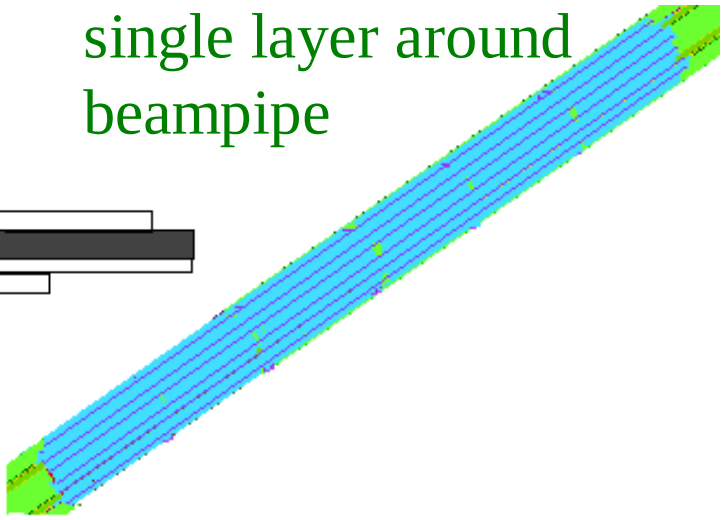
Feb 22, 2001 meeting

Described in RunIIb Silicon Working Group document submitted to PAC: CDF note 5425

L00 replacement: single layer around beampipe



ATLAS style sensor
FPIX readout chip



PAC comments:

The possibility of using pixels in the innermost layer is an intriguing option mentioned by both collaborations. The Committee urges them to work closely with the Fermilab pixel group, building on the success of this R&D program.

Overview

- Replace Layer00 strips with pixels
  - radiation survivability to 30 Mrad / 30 fb-1 is desirable
  - pattern recognition: 3.3 M channels vs 14 K channels
  - z resolution 120 μm possible
  - large S:N helps r-ϕ resolution, trigger, etc.
  - keep Layer00 strip option a fallback
- Pixels can be ready for 2004
  - ATLAS sensors are in production
    - Two vendors: Cis and Tesla
    - Sally Siedel (UNM-CDF/ATLAS) leads ATLAS sensor group and will do sensor probing
    - Coordinating non-disclosure/patent agreements
    - Engineering available in March to make CDF design
  - FPIX readout chip final prototype (pre-FPIX2Tb) works!
    - Radiation qualified to >30 Mrads (Co-60 + protons)
    - SEU radiation testing at IU cyclotron this Spring
    - Only the periphery needs to be defined
    - BTeV requirements for chip @ 6 mm exceed our requirements – still possible for chips to be identical.
- Overlap with BTeV and D0
  - BTeV 10% scale test is comparable
  - Good communication with D0 pixel interest

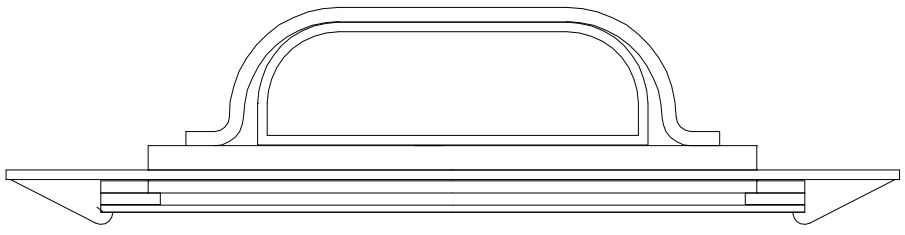
FY01 Requests

- Mechanical
  - ENGINEERING SUPPORT
  - System level mock-up
  - Prototype stave
  - Cooling test (highest priority)
- Electronics
  - ENGINEERING SUPPORT
  - DAQ test stand
  - Progress with RHVD R&D

Item	Estimated Cost k$	Contingency	Total Costs
DAQ Test stand	15	7.5	22.5
System Mechanics	20	10	30
Staves prototypes	20	10	30
Cooling	15	7.5	22.5
Total M&S	70	35	105
Mech. Engineering (FTE)	1.0	0.5	1.5
ESE	0.5	0.25	0.75
Design	1.0	0.5	1.5
Technician	1.0	0.5	1.5

Mechanical Progress

- Mike Hrycyk (SiDet)
  - CERN visit with ATLAS project engineers
  - 3D modeling shows difficult geometry
  - Some preference for carbon fiber shell
  - Pixels should be integrated with the rest of RunIIb replacement silicon
  - Pixels as the only RunIIb replacement is a undesirable, separate, and non-trivial project
- Possible new chip geometry
  - 128 rows x 22 columns (was 160 row x 18 col)
  - Driven by BTeV considerations
  - Lots of flexibility: 12-fold vs 8-fold geometry; inner or next-to-inner layer



Cooling

- ATLAS cooling is aggressive and has had about 5 yrs of R&D
- Updated power budget is ~500W (40-50 W/stave) for pixel system
  - Readout chips: 288 W
  - Leaky sensors: 86 W (after rad damage)
  - Data lines (1 ohm): 24 W (max)
  - Power lines: 45-140 W (max)
- Goal was use current CDF cooling system (H_20-glycol)
- Greg Derylo (SiDet) has performed some initial calculations
  - Laminar flow of current system prevents heat flow into coolant. T~20C
  - Other options such as the fluorocarbon that CMS will use look promising
- A cooling test is useful in its own right for this and for future projects

DAQ

- Carnigie Mellon, Johns Hopkins, FNAL ESE, UC Davis, and Rad Hard Vertex groups involved.
- Engineer supported beginning in May – expert in FPGA design
- Two basic options
  - Low speed transmission directly from FPIX to DAQ
  - High speed transmission to a port card
  - Token scheme would simplify HDI
- Pixel-FIB board looks straight forward – FPGAs are powerful.
- ESE group has developed a PC based pixel test stand.

Physics Studies

- Work in progress at LBNL
- Much can be done parametrically

Cost

Estimate of $1.5M still holds until more of a detailed design is done. If CDF/D0/BTeV share costs, then estimate $1M for CDF's share. Half would be needed in FY02 and half in FY03.

Schedule

Critical path is chips and sensors – both of these are on track to be ordered in early FY02. Module production could begin in June 2002 with mech. and DAQ design in parallel. System assembly in early 2003. Add 6 months contingency for 2004.

Summary

Pixels are a viable technology for RunIIb. We require strong support to achieve the schedule. In the end, the physics justification needs further clarification and pixels should be considered in the context of best achieving the physics goals of an entire RunIIb effort.